IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:

Baker

Serial No.: 09/061,017

Filed: April 15, 1998

For: METHOD AND APPARATUS FOR INTERLEAVING A DATA STREAM

Art Unit: 2732

Examiner: D. Vincent

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereafter "Appellant") hereby submits this Brief, in triplicate, in support of his Appeal from a final decision by the Examiner in the above-captioned case. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application (hereinafter "application").

An oral hearing is not desired.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on:

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal, which will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-19 are currently pending in the application. No claims have been cancelled or added. Claims 1-19 were rejected in the Final Office Action mailed on August 19, 1999 and are the subject of this appeal. A Response after Final Action was mailed on October 19, 1999, in which no claims were amended. The Examiner confirmed his final rejection in an Advisory Action mailed on November 2, 1999.

Claims 1-3, 6-9 and 11-19 stand rejected under U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,291,485 by Afify et al. ("Afify"). Claims 4, 5 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Afify as applied to claim 1, and further in view U.S. Patent No. 5,825,772 by Dobbins et al. ("Dobbins").

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on August 19, 1999 and the Advisory Action mailed on November 2, 1999, in which claims 1-19 were rejected, Appellant timely filed a Notice of Appeal on November 19, 1999.

A copy of all claims on appeal, claims 1-19, is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

It is sometimes desirable to insert and/or remove consecutive binary digital signals, referred to in this context as groupings of bits, from a data stream. Likewise, although the invention is not limited in scope in this respect, it may be desirable to interleave two data streams to form a single data stream. In another example, although, again the invention is not limited in scope in this respect, it may be desirable to insert or remove a virtual local area network (VLAN) tag from a data stream, such as in the context of an Ethernet switch or similar device, for example. Specification, page 3, lines 12-17.

FIG. 1 is a block diagram illustrating an embodiment, 100, of a circuit for interleaving a data stream in accordance with the present invention, although this is just one example embodiment and, of course, the invention is not limited in scope to this particular embodiment. As illustrated in FIG. 1, binary digital signals or bits traverse a data bus 185. In this particular embodiment, a sequence of groupings of bits from a data stream are received and written from data bus 185 into memory 110. In this particular embodiment, the groupings have a predetermined size, such as a byte. Memory 110 comprises a first-in, first-out memory (FIFO). As illustrated in FIG. 1, FIFO memory 110 includes a FIFO read pointer 105 and a FIFO write pointer 115. These may be employed to write received groupings of bits from the data stream into the FIFO memory and to read groupings of bits from the FIFO memory and apply them to multiplexor (MUX) 120, as shall be explained in more detail hereinafter. Specification, page 3 lines 24-25, 29-32 and 34 to page 4, line 4; FIG. 1.

In embodiment 100, the read and write pointers of FIFO 110 may be employed to effectively skip or extract received groupings of bits from the data stream that has been stored in the FIFO. For example, once a grouping of binary digital signals, for example, a byte, has been written to FIFO 110, read pointer 105 may skip that grouping so that it is not read from FIFO 110 and applied to MUX 120. As illustrated in FIG. 1, a state machine 150 provides the signals to FIFO read pointer 105 so that this extraction operation may be accomplished, for this embodiment. Likewise, as illustrated, state machine 150 also provides signals to MUX ports 125, 135, 145 as well, to ensure that the operations occurring at MUXes 120, 130 and 140 are coordinated with the operation of FIFO 110 when this extraction operation is performed. Specification, page 4, lines 5-13; FIG. 1.

In embodiment 100, selected groupings of bits from the data stream, stored in the FIFO, are read from the FIFO or applied to MUX 120. As illustrated in FIG. 1, in this particular embodiment, this operation is performed a grouping at a time. Therefore, a grouping of binary digital signals, such as a byte, is applied to MUX 120, all the bits being applied to input ports of the MUX substantially simultaneously. One advantage of employing this approach is that it allows the use of a slower speed FIFO while supporting a high output clock rate. More particularly, in this embodiment, although bits may be received at a relatively high rate by a data bus 185, because groupings of bits are read from FIFO 110, more time separates read operations, permitting a relatively slower memory. Specification, page 4, lines 16-24, FIG. 1.

Embodiment 100 also includes the capability to interleave a grouping or groupings of binary digital signals. In this particular embodiment, this capability is provided via the arrangement between MUXes 120, 130 and 140, as explained in more detail hereinafter. As

illustrated in FIG. 1, the output data stream is produced at output port 165 of MUX 140. Signals are applied to the input ports of a MUX, 140 in this particular embodiment, from the output ports of MUXes 120 and 130, respectively. Likewise, a signal applied to MUX select port 145 of MUX 140 controls which of the input signals applied to MUX 140 appears at its output port 165. Specification, page 4, lines 26-32; FIG. 1.

In this embodiment, 100, MUX 130 receives input signals from an alternative data source. This data source or data stream is to be interleaved with the data stream written to FIFO 110, as previously described. Therefore, a signal applied to MUX select port 135 of MUX 130 controls the application of signals from this alternative data source or data stream to MUX 140. Likewise, selective groupings stored in FIFO 110 may be applied to the input port of 140 via MUX 120 by the application of a control signal to MUX select port 125 of MUX 120. Therefore, as previously illustrated, in this particular embodiment, controlling the signals applied to MUX select ports 125, 135 and 145 of MUXes 120, 130 and 140 may result in the interleaving of the data stream written to FIFO 110 and the data stream applied to MUX 130. The alternative data stream or data source applied to MUX 130 may comprise bits or binary digital signals representing a VLAN tag, for example. Therefore, this tag may be interleaved with the data signals with FIFO 110, as a data stream is produced by output port 165. Specification, page 4, line 33 to page 5, line 11; FIG. 1.

VI. ISSUES PRESENTED

A. Whether claims 1-3, 6-9 and 11-19 are patentable over Afify under 35 U.S.C § 103(a).

B. Whether claims 4, 5 and 10 are patentable over Afify in view of Dobbins under 35 U.S.C. § 103(a).

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1-3, 6-9 and 11 stand or fall together as Group I;

Claims 12-19 stand or fall together as Group II;

Claims 4, 5 and 10 stand or fall together as Group III;

Reasons for separate patentability of the above-indicated Claim Groups I-III are presented in the argument section pursuant to 37 C.F.R. §1.192(c)(5).

VIII. ARGUMENT

A. **REJECTION OF CLAIMS 1-3, 6-9 and 11 (GROUP I), AND 12-19 (GROUP II) UNDER 35 U.S.C. § 103 AS BEING UNPATENTABLE OVER AFIFY IS IMPROPER. AFIFY DOES NOT RELATE, NOR IS IT ANALOGOUS, TO INTERLEAVING A DATA STREAM. FURTHERMORE, THE EXAMINER HAS ENGAGED IN PROSCRIBED HINDSIGHT ANALYSIS. ADDITIONALLY, AFIFY DOES NOT TEACH OR SUGGEST INTERLEAVING A DATA STREAM.**

The Examiner has rejected claims 1-3, 6-9 and 11-19 under 35 USC § 103(a) as being unpatentable over Afify. As is well-settled, in order to support a rejection under this statutory provision, the patent(s) cited by the Examiner must be related to the claimed subject matter. See e.g. In re Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). ("[W]hether a combination of known elements would have been obvious to one of ordinary skill in depends on various factors, including whether the elements exist in 'analogous art', that is, art that is reasonably pertinent to the problem with which the inventor is concerned.") There are many reasons why Afify is not "analogous" or "reasonably pertinent" to the claimed subject matter, such as claim 1, for example. Therefore, Applicants respectfully assert that the Examiner has not met his burden in showing that the cited patent renders obvious claim 1, or the remaining claims, as shall be explained in more detail below.

Furthermore, even were Afify analogous or pertinent to the subject matter of these claims, such as claim 1 as an example, which Appellant opposes, the rejection by the Examiner would be still be improper because it is based on hindsight reconstruction analysis. This type of analysis is inappropriate and has been consistently proscribed by the Federal Circuit. See e.g. In re Gorman at 1888. ("It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps.") Appellant also addresses this assertion in more detail below.

Furthermore, as is also well-settled, to support a rejection under this statutory provision, the Examiner must demonstrate that the cited patent, namely Afify, teaches or suggests the claimed invention to one of ordinary skill in the art. See e.g., In re Lueders, 42 USPQ2d 1481, 1482 (Fed. Cir. 1997) ("This legal conclusion, however, rests on several factual findings, including among others, what a prior art reference teaches or suggests – two different inquiries...") Here, even were Afify a proper reference and the Examiner's rejection not based on hindsight analysis, which Appellant also opposes, the rejection by the Examiner would still be

improper as one of ordinary skill in the art having Afify before him or her would still not be able to produce the invention are recited in claim 1, for example. Appellant, of course, addresses these assertions in more detail hereafter.

1. Claim Group I

As indicated above, it is respectfully asserted that the Examiner, in supporting his rejection under 35 U.S.C § 103(a), has failed to establish that the cited patent, Afify, renders the claimed invention, in particular claim 1, obvious. In this regard, Claim 1 of the application states:

> A method of interleaving a data stream comprising:
> writing a sequence of groupings of bits from the data stream, the groupings having a predetermined size, from a data bus into a memory;
> applying selected groupings read from the memory to a first multiplexer (MUX);
> applying the groupings applied to the first MUX to a second MUX; and
> applying at least one grouping to the second MUX between applying groupings from the first MUX to the second MUX.

Applicant respectfully asserts that the cited patent is not analogous to or reasonably pertinent to the subject matter of claim 1. Specifically, in this regard, Appellant noted in his response mailed on August 6, 1999 that there are many reasons why the cited patent does not render claim 1 obvious. For example, **Afify has nothing to do with interleaving a data stream**. Additionally, **Afify does not "apply[ing] at least one grouping to [a] second MUX between applying groupings from [a] first MUX to the second MUX**."

Comparing claim 1 to the cited patent will illustrate that the specific aspects of claim 1 indicated above are not taught or suggested by Afify. However, these are just examples to show that Afify does not at all relate to the invention as recited, for example, in claim 1. In column 3, lines 6-9 of Afify, which is specifically cited by the Examiner, Afify states, "According further to the present invention, virtual tributaries of one size can be translated for interpretation according to a method for interpreting virtual tributaries of another size."

As previously stated, Afify is not related to the subject matter of claim 1 and, therefore, not a proper reference. The legal test for analogous and pertinent subject matter is well-settled, and has been consistently applied by the Federal Circuit in determining patentability under 35 U.S.C. § 103. The standard that has been applied by the court is twofold. First, it is determined whether the patent is within the field of the inventor's endeavor. Second, if it is not within the field of endeavor, it must be determined if the patent is reasonably related to the particular problem facing the inventor. See e.g., In re Deminski, 230 USPQ 313, 315 (Fed. Cir. 1986).

Under this test, Appellant respectfully asserts that the cited patent does not meet the above standard.

Under the first prong of the test, Appellant respectfully asserts that the patent cited by the Examiner is not within the field of Applicant's endeavor. One of ordinary skill in the art, in the course of solving the problem of interleaving data streams, for example, would not look to the art of synchronous optical network virtual tributary translation. **Claim 1 in no way relates to virtual tributaries or synchronous optical networks and, therefore, Afify cannot be considered to be within the field of Applicant's endeavor.** In this respect, the Federal Circuit has held that art is not in the same field of endeavor merely because is relates to similar subject matter. See e.g. Wang Laboratories, Inc. v. Toshiba Corp., 26 USPQ2d 1767, 1773 (Fed. Cir. 1993). ("The Allen-Bradley art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories. It involves memory circuits in which modules of varying sizes may be added or replaced; in contrast the subject patents teach compact memory modules.")

In this regard Afify specifically states in column 2, lines 58-65:

> An object of the present invention is to **translate virtual words in one format to virtual words in another format**.
>
> According to the present invention, **virtual words in one format may be translated to virtual words in another format** by encode/decode means, responsive to data signals of a second/first VT size, for providing the data signals as data formatted for the first/second VT size.

In contrast the specification of the application, in discussing Fig. 1 of the drawings, specifically states on page 4, lines 5-7 and 25-27:

> As illustrated in FIG. 1, the read right pointers of FIFO 11 may be employed to effectively **skip or extract received groupings** of bits from the data stream that has been stored in the FIFO.
>
> [T]his particular embodiment of a circuit for interleaving a data stream includes the capability to **interleave a grouping or groupings** of binary digital signals.

Comparing the cited portions of Afify and the application demonstrates that Afify does not at all relate to extracting or interleaving groups of bits as described in the specification of the application. **Therefore, Appellant respectfully asserts that Afify is not in the same field of endeavor as claim 1 merely because it relates to data formatting. That patent is directed to virtual tributary translation in synchronous optical networks; in contrast claim 1 teaches, for example, interleaving data streams.**

Under the second prong of the test, Applicant respectfully asserts that the cited patent is also not pertinent to the particular problem addressed by claim 1. In this respect, Judge

Lourie's comments in Wang Laboratories at 1773 are illustrative. In that case, Judge Lourie specifically stated:

> A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem. (citation omitted)

In that case, the prior art was an Allen-Bradley memory module for use in industrial control computers. That art was found to not be reasonably pertinent to a compact memory module for use in personal computers, the subject matter of the Wang patents. Here, the court felt that because the Allen-Bradley art was specifically for use in larger, more expensive industrial computers, there was sufficient evidence to support a finding that it was not reasonably pertinent to Wang's memory modules for use in a personal computer. Likewise, Afify specifically states in column 1, lines 41-46:

> The signals used to interface between network elements are operating... according to ANSI standard T1.105 entitled "Digital Hierarchy Optical Interface Rules and Format Specifications."

In contrast, the specification of the application states on page 3, lines 26-28:

> [A] system may include a personal computer (PC) adapted to be coupled to an [E]thernet compliant network, for example.

Although the invention is not limited in scope to the Ethernet, it is noted that the Ethernet standard is well known. Comparing the quoted portions of Afify and the application shows that at least this particular embodiment is directed to a different standard. Therefore, Appellant respectfully asserts that Afify, being directed to ANSI standard T1.105, would not commend itself to one addressing the problem of interleaving data streams, such as in a system that is compliant with the Ethernet standard or any similar data stream standard. Because Afify is directed specifically to virtual tributary transformation in ANSI compliant synchronous optical networks, it is not reasonably pertinent to interleaving a data stream as described in the application, for example.

Based on the foregoing, **Appellant respectfully asserts that transformation of virtual tributaries in a Synchronous Optical Network, which is what the Afify patent as a whole is directed to, is not analogous to a method for interleaving a data stream as recited in claim 1. Furthermore, the cited patent is not reasonably pertinent to the subject matter of claim 1, as one of ordinary skill in the art would not look to a patent in this art to address the problem of interleaving a data stream.** Therefore, the Examiner has not met his burden in this respect.

Notwithstanding Appellant's assertion in the response mailed on August 6, 1999 that Afify does not at all relate to the subject matter of claim 1 the Examiner stated, in the Final Action that:

> [A]fify clearly discloses writing a sequence of groupings of bits from a data bus into memory (see i.e. 114, 122, 110, Fig. 9 or 114, 118 and 110, Fig. 10), applying groupings to a first MUX (i.e. 126 or 132, Fig. 9 or 194, Fig. 10), applying groupings to a second MUX (i.e., 132, Fig. 9 or 194, Fig. 10) and applying "at least one" grouping to the second MUX between applying groupings from the first MUX to the second MUX (see Fig. 9 where the same data is going to the second MUX and the OHMUX and not how Overhead (OH) data is interleaved into the main data). With this in mind, it is not understood how the Applicant could possibly argue that Afify does not relate at all to the subject.

Even if, contrary to Appellant's position, the Board were to determine that Afify is analogous art, which, as discussed above, Appellant respectfully asserts that it is not, this rejection by the Examiner would still be improper. As was previously indicated, the portion of the Examiner's comments cited above represents impermissible hindsight analysis. On this point, Judge Newman's comments in In re Gorman at 1888 are instructive. That case deals with whether a *prima facie* case of unpatentability has been established under 35 U.S.C. § 103(a) and is, therefore, relevant here. Judge Newman stated, in part:

> As in all determinations under 35 U.S.C. §103, the decisionmaker must bring judgment to bear. It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. (citation omitted)

Appellant respectfully asserts that the Examiner, as shown by the above quoted excerpt from the Final Action, has "engage[d] in a hindsight reconstruction of the claimed invention." **In taking claim 1 and merely associating its elements with elements from the figures of Afify, the Examiner has used Appellant's "structure as a template and select[ed] elements from [Afify] to fill the gaps." Appellant respectfully asserts that this analysis by the Examiner does not show how Afify "provide[s] some teaching whereby [claim 1] would have been obvious."** For example, the Examiner has merely associated the language "writing groupings of bits" and "applying groupings" with elements of Figs. 9 and 10 of Afify with no indication of how Afify suggests or teaches interleaving a data stream, as recited in claim 1. By merely reciting portions of claim 1 and then selecting corollary elements in Afify, the Examiner has not brought "judgment to bear." Therefore, the Examiner has failed to establish a prima facie case of unpatentability under 35 U.S.C. § 103(a) under this standard.

Additionally, even were the Board to determine that Afify is analogous art and the Examiner's rejection is not based on hindsight reconstruction, which, as previously discussed,

Appellant asserts is not correct, the Examiner's rejection would, nonetheless, still be improper. One of ordinary skill in the art, having the Afify patent before him or her, would still be unable to produce the invention as recited in claim 1. In other words, Afify does not teach the invention as recited in claim 1.

It is well settled that in order establish a *prima facie* case of obviousness the teachings of the prior art must suggest the claimed invention to one of ordinary skill in the art. The Federal Circuit has addressed this principle in a number of cases, for example in In re Bell, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993), the court specifically stated:

> "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." (citation omitted)

Applicant respectfully asserts that the patent cited by the Examiner, Afify, fails to establish a *prima facie* case of obviousness.

In this regard, the teachings of Afify would not suggest the subject matter of claim 1 to one of ordinary skill in the art. **The portions of that patent cited by the Examiner, and the patent as a whole, do not relate to interleaving a data stream as recited in claim 1.** The problem at which Afify is directed is stated in column 3, lines 52-54, which specifically states "the problem may be stated as how to translate virtual words from one format to virtual words in another format." **Since the teachings of Afify are directed to converting virtual words from one virtual tributary format into another virtual tributary format in a synchronous optical network, that patent does not teach interleaving a data stream as recited, for example, in claim 1.** The problem solved by Afify, translating virtual words, is not even analogous to the problem solved by the application, interleaving data streams, as has been previously described in detail.

Based on the foregoing, Appellant respectfully asserts that claim 1 patentably distinguishes from the cited patent, namely Afify. Therefore, the Examiner's rejection of that claim under 35 U.S.C. § 103(a) is improper. Furthermore, because claims 2, 3, 6-9 and 11 depend from claim 1, these claims include all the limitations of claim 1. It is respectfully asserted that these claims patentably distinguish from Afify on the same basis as claim 1. Therefore, Appellant respectfully submits that claims 1-3, 6-9 and 11 (Group I) recite patentable subject matter.

2. Claim Group II

As previously indicated, Claim Group II includes claims 12-19. In the Final Office Action, mailed on August 19, 1999, the Examiner rejected these claims on the same basis as his rejection of Claim Group I under 35 U.S.C. § 103(a). As was indicated by the remarks made above with regard to Claim Group I, the Examiner has failed to establish a *prima facie* case under this statutory provision. Claims 12 and 18, the independent claims of Claim Group II, are drawn, respectively, to an apparatus, and a system, capable, for example, of executing embodiments of methods of Claim Group I. It is noted that Claim Group II is, of course not limited in scope to executing embodiments of methods as recited in Claim Group I and Appellant does not intend to limit the scope of Claim Group II in this respect. Nonetheless, Appellant's arguments with respect to Claim Group I apply similarly to Claim Group II, and are incorporated by reference in this subsection of the Appeal Brief.

B. **REJECTION OF CLAIMS 4, 5 and 10 (GROUP III), UNDER 35 U.S.C. § 103 AS BEING UNPATENTABLE OVER AFIFY IN VIEW OF DOBBINS IS IMPROPER. THE EXAMINER HAS NOT PROVIDED THE NECESSARY SUGGESTION OR MOTIVATION TO MAKE THE ASSERTED COMBINATION. FURTHERMORE, AFIFY IS NOT RELATED, NOR ANALOGOUS, TO INTERLEAVING A DATA STREAM. THEREFORE, ONE OF ORDINARY SKILL WOULD BE UNABLE TO PRODUCE THE CLAIMED INVENTION, EVEN WERE THEY TO MAKE THE COMBINATION.**

The Examiner has rejected claims 4, 5 and 10 (Group III) as being unpatentable over Afify as applied to claim 1 above, and further in view of Dobbins. In his rejection made in the Office Action mailed on May 11, 1999, which he further confirmed in the Final Office Action mailed on August 19, 1999, the Examiner relies on Dobbins for teaching the limitation of VLAN tags of these claims. In this regard, the Examiner merely states, "However, Afify fails to particularly call for the VLAN tags. As shown in Figs. 3-4, Dobbins teaches VLAN tags." Therefore, the Examiner concedes that Afify does not teach VLAN tags.

Even were the combination asserted by the Examiner to produce the invention as recited in claim 4, as an example, which Appellant asserts it does not, the Examiner has not provided the necessary suggestion or motivation to make the asserted combination. The Federal Circuit has consistently applied this requirement. See e.g., In re Gorman at 1888 ("When it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation in the prior art to make the selection

made by the applicant.") As was previously indicated, Afify is directed to virtual tributary translation in an ANSI standard T1.105 compliant synchronous optical network. Dobbins is directed to packet switched data communication networks. The abstract of that patent specifically states that the invention is a:

> Method and apparatus providing connection-oriented services for packet switched data communications networks.

Because Afify is directed to an optical network standard and Dobbins is directed to packet switched networks, the combination asserted by the Examiner lacks the necessary suggestion or motivation for one of ordinary skill in the art to make to the combination, even were the combination to produce the invention as recited in claim 4, for example, which Appellant asserts that it does not.

Furthermore, at least in part, because the Examiner is incorrect in his characterization of the Afify patent, this rejection is improper. It is respectfully asserted that the Examiner has failed to meet his burden of establishing a *prima facie case* of unpatentability under 35 U.S.C. § 103, as required, for example, by In re Lueders, 42 USPQ2d 1481 (Fed. Cir. 1997). Even assuming, without conceding, that the combination asserted by the Examiner is proper, nonetheless, because, as previously explained with respect to Claim Group I, the Afify patent does not relate, nor is it analogous to the subject matter of these claims. The arguments made above with respect to claim 1 apply similarly here. **Therefore, in this regard, the combination asserted by the Examiner would not teach, suggest or render obvious interleaving a data stream as recited, for example, in claim 1.** It is noted that the claims of Claim Group III depend from and, therefore, include all of the limitations of claim 1. Likewise, the Dobbins patent also does not relate to interleaving data streams and is relied on by the Examiner solely for its treatment of VLAN tags. **Therefore, one of ordinary skill in the art having these two patents before him or her would not be able to produce the invention as recited in claim 4, for example.**

Finally, as previously stated, the main patent cited by the Examiner, namely Afify, is not related, nor is it analogous, to the claimed subject matter, as was previously discussed in detail. Under these circumstances, **the combination would not render the claimed subject matter obvious as one of ordinary skill in the art would not look to Afify in solving the particular problem addressed by Appellant.** Based on the foregoing, it is respectfully asserted that claims 4, 5 and 10 recite patentable subject matter.

IX. CONCLUSION

Appellant respectfully submits that all the pending claims in this application are patentable and requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $300.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c) and a check for $110 to cover the fee for a one month extension of time for one other than a small entity as specified in 37 C.F.R. § 1.17(a). Please charge any shortages and credit any overcharges to Deposit Account No. 02-2666.

Respectfully submitted,

Date: 1/25/00

Howard A. Skaist
Attorney for Appellant
Registration Number: 36,008

Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

X. APPENDIX A: CLAIMS ON APPEAL

1. A method of interleaving a data stream comprising:

writing a sequence of groupings of bits from the data stream, the groupings having a predetermined size, from a data bus into a memory;

applying selected groupings read from the memory to a first multiplexer (MUX);

applying the groupings applied to the first MUX to a second MUX; and

applying at least one grouping to the second MUX between applying groupings from the first MUX to the second MUX.

2. The method of claim 1, wherein the memory comprises a first-in, first-out memory (FIFO).

3. The method of claim 1, wherein each of the groupings comprises a byte.

4. The method of claim 1, wherein said at least one grouping comprises bits representing a virtual local area network (VLAN) tag.

5. The method of claim 4, wherein said at least one grouping comprises bits originating from another data stream.

6. The method of claim 1, wherein writing a sequence of groupings of bits into a memory comprises receiving a consecutive sequence of groupings of bits and writing the consecutive sequence into the memory.

7. The method of claim 6, wherein receiving a consecutive sequence of groupings of bits and writing the consecutive sequence into the memory comprises receiving bursts of data signals and writing the received bursts of data signals to the memory.

8. The method of claim 6, wherein the bursts of data signals are provided via the data bus from at least one burst-mode memory.

9. The method of claim 8, wherein the at least one burst mode memory comprises at least one burst mode dynamic random access memory (DRAM).

10. The method of claim 1, wherein applying selected groupings read from the memory to a first MUX comprises selecting, from the stored groupings, groupings that represent signal information other than a virtual local area network (VLAN) tag.

11. The method of claim 1, wherein applying groupings read from memory to the first MUX occurs a grouping at a time.

12. An integrated circuit (IC) comprising:

a memory, a plurality of multiplexers (MUXes), and a state machine;

said memory, MUXes and state machine being coupled so that, responsive to applied control signals, selected groupings of bits from a received bit stream are capable of being extracted to produce another bit steam different from the received bit stream.

13. The IC of claim 12, wherein said state machine comprises a memory extraction state machine.

14. The IC of claim 12, wherein said memory comprises a first-in, first-out memory (FIFO).

15. The IC of claim 12, wherein said memory and MUXes are further coupled so that, responsive to additional applied control signals, at least one selected grouping from another data stream may be inserted to produce a bit stream different from the received bit stream.

16. The IC of claim 15, wherein said memory comprises a first-in, first-out memory (FIFO), and said state machine comprises a FIFO extraction state machine.

17. The IC of claim 15, wherein said memory is adapted to receive said received bit stream in bursts of data signals.

18. A system comprising: a computer adapted to be coupled to an ethernet compliant network; said computer including an integrated circuit; the integrated circuit comprising a memory, a plurality of multiplexers (MUXes) and a state machine; said memory, MUXes, and state machine being coupled so that, responsive to applied control signals, selected groupings of bits from a received bit stream are capable of being extracted to produce another bit stream different from the received bit stream.

19. The system of claim 18, wherein said memory and MUXes are further coupled, so that, responsive to additional control signals, at least one selected grouping from another data stream may be inserted to produce yet another bit stream different from the received bit stream.